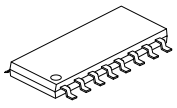
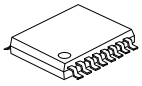
U74HC4060

CMOS IC

14-STAGE ASYNCHRONOUS BINARY COUNTERS AND OSCILLATORS



SOP-16



TSSOP-16

QFN-16(3.5×2.5)

■ DESCRIPTION

The **U74HC4060** are high-speed Si-gate CMOS device.

The **U74HC4060** devices consist of an oscillator section and 14 ripple-carry binary counter stages. The oscillator configuration allows design of either RC or crystal oscillator circuits with three oscillator terminals (CLKI, $\overline{CLKO}$, CLKO) , ten buffered outputs (Q_D to Q_J and Q_L to Q_M) and an overriding asynchronous master reset (CLR) . The oscillator may be replaced by an external clock signal at input CLKI. In this case keep the other oscillator pins ($\overline{CLKO}$, CLKO) floating. The counter advances on the negative-going transition of CLKI. A high level at the clear (CLR) input disables the oscillator and resets the counter to zero (all Q output low).

■ FEATURES

* Operate from 2.0V to 6.0V
* Low Input Current:0.1μA
* Outputs Can Drive Up To 10 LSTTL Loads
* Low Power Consumption, 8μA Max. I_{CC}
* 4mA Output Drive at 5V
* Allow Design of Either RC or Crystal Oscillator Circuits

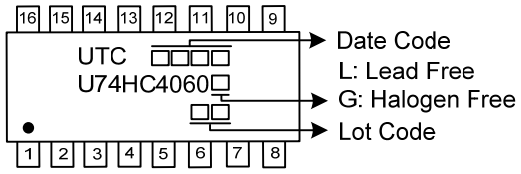
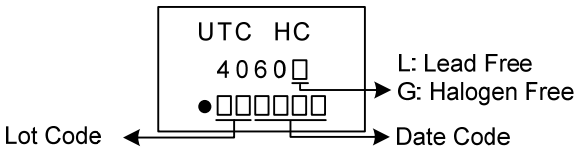
■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74HC4060L-S16-R	U74HC4060G-S16-R	SOP-16	Tape Reel
U74HC4060L-P16-R	U74HC4060G-P16-R	TSSOP-16	Tape Reel
U74HC4060L-QAH-R	U74HC4060G-QAH-R	QFN-16(3.5×2.5)	Tape Reel

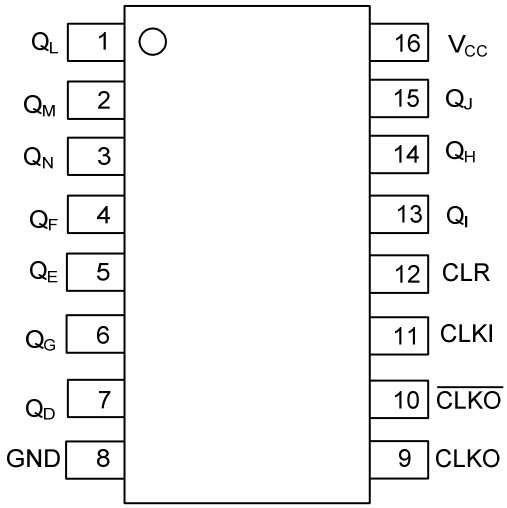
U74HC4060G-S16-R
(1)Packing Type
(2)Package Type
(3)Green Package

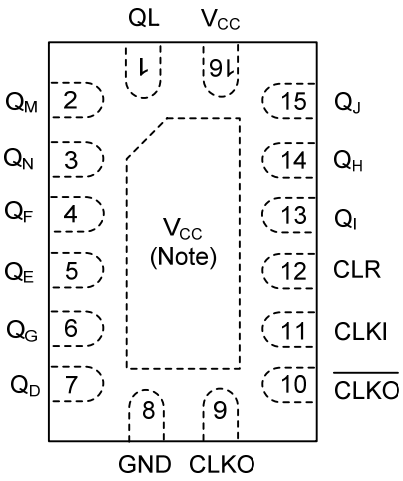
(1) R: Tape Reel
(2) S16: SOP-16, P16: TSSOP-16
QAH: QFN-16(3.5×2.5)
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

SOP-16 / TSSOP-16	QFN-16(3.5×2.5)
	

■ PIN CONFIGURATION





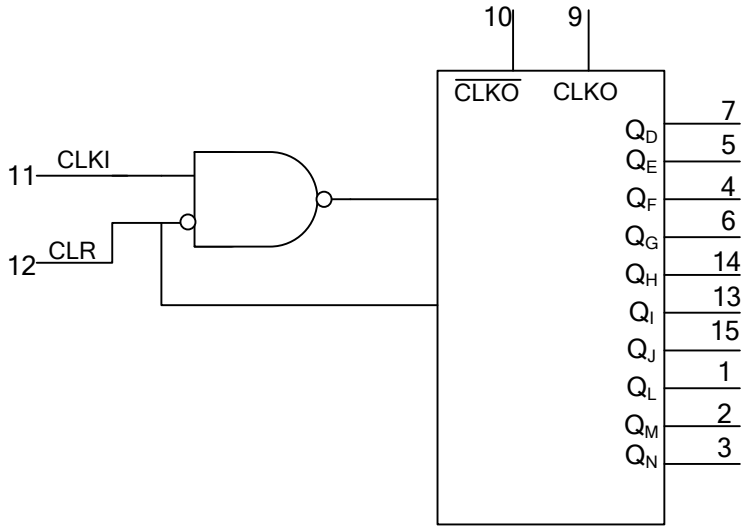
Note: This pad pin cannot be used as a supply pin. The product's chip substrate is attached to the package pad frame through an adhesive. If the pad need to be soldered, it should be connected to V_{CC} or remaining floating.

■ FUNCTION TABLE

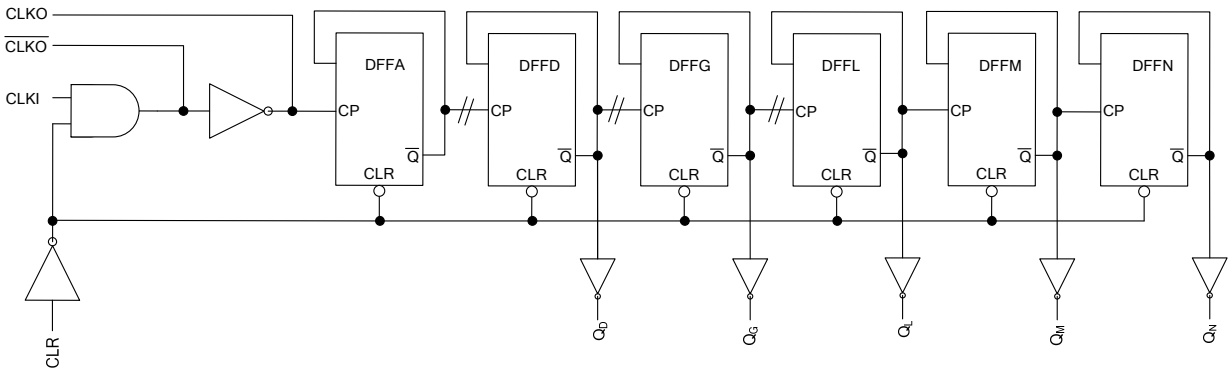
INPUTS		FUNCTION
CLK	CLR	
↑	L	No change
↓	L	Advance to next stage
X	H	All outputs L

Note: H: HIGH voltage level
L: LOW voltage level
X: Don't care. High impedance OFF-state
↑: Low-to-High CP transition
↓: High-to-Low CP transition

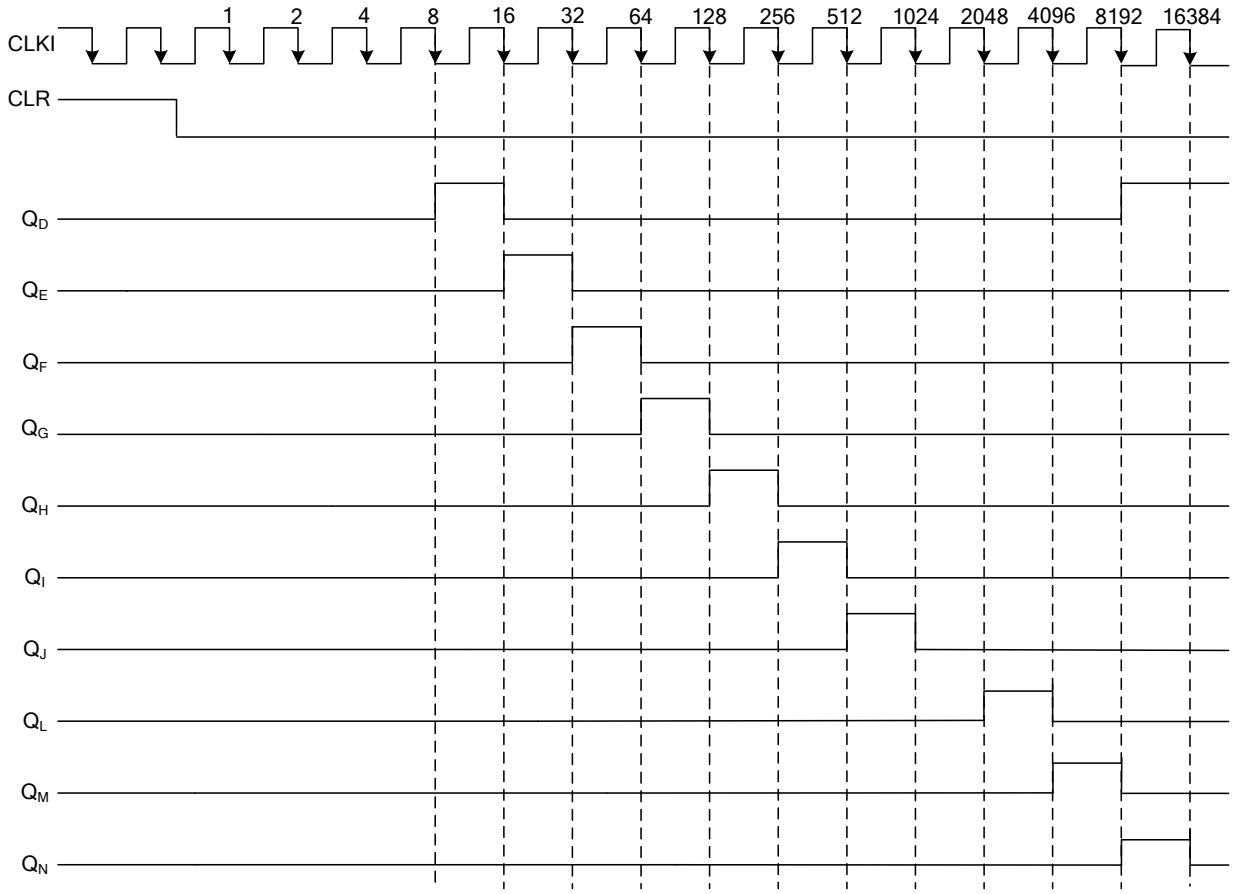
■ LOGIC SYMBOL



■ LOGIC DIAGRAM



■ TIMING DIAGRAM



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CC}		-0.5 ~ 7.0	V
Input Clamp Current	I_{IK}	$V_I<0$ or $V_I>V_{CC}$	±20	mA
Output Clamp Current	I_{OK}	$V_O<0$ or $V_O>V_{CC}$	±20	mA
V_{CC} or GND Current	I_{CC}		±50	mA
Continuous Output Current	I_{OUT}	V_O=0 to V_{CC}	±25	mA
Storage Temperature	T_{STG}		-65 ~ + 150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING CONDITIONS (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}	Operating	2.0		6.0	V
Input Voltage	V_{IN}		0		V_{CC}	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Rise or Fall Times	t_R, t_F	V_{CC}=2.0V			1000	ns
		V_{CC}=4.5V			500	ns
		V_{CC}=6.0V			400	ns
Operating Temperature	T_A		-40		+125	°C

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-Level Input Voltage	V_{IH}	V_{CC}=2V	1.5			V
		V_{CC}=4.5V	3.15			V
		V_{CC}=6V	4.2			V
Low-Lever Input Voltage	V_{IL}	V_{CC}=2V			0.5	V
		V_{CC}=4.5V			1.35	V
		V_{CC}=6V			1.8	V
High-Level Output Voltage	V_{OH}	V_{CC}=2V, I_{OH}=-20μA	1.9	1.998		V
		V_{CC}=4.5V, I_{OH}=-20μA	4.4	4.499		V
		V_{CC}=6V, I_{OH}=-20μA	5.9	5.999		V
		V_{CC}=4.5V, I_{OH}=-4mA	3.98			V
		V_{CC}=6V, I_{OH}=-5.2mA	5.48			V
Low-Level Output Voltage	V_{OL}	V_{CC}=2V, I_{OL}=20μA		0.002	0.1	V
		V_{CC}=4.5V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=6V, I_{OL}=20μA		0.001	0.1	V
		V_{CC}=4.5V, I_{OL}=4mA			0.26	V
		V_{CC}=6V, I_{OL}=5.2mA			0.26	V
Input Leakage Current	$I_{I(LEAK)}$	V_{CC}=6V, V_{IN}= V_{CC} or GND			±100	nA
Quiescent Supply Current	I_{CC}	V_{CC}=6V, V_{IN}=V_{CC} or GND, I_{OUT}=0			8	μA

■ TIMING REQUIREMENTS (T_A=25°C, unless otherwise specified)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Clock Frequency		f_{clock}	V_{CC}=2V			4.3	MHz
			V_{CC}=4.5V			22	MHz
			V_{CC}=6V			25	MHz
Pulse Duration	C_{LKI} High or Low	t_W	V_{CC}=2V	115			ns
			V_{CC}=4.5V	23			ns
			V_{CC}=6V	20			ns
	C_{LR} High		V_{CC}=2v	115			ns
			V_{CC}=4.5V	23			ns
			V_{CC}=6V	20			ns
Setup time, C_{LR} Inactive Before C_{LKI} High To Low		t_{su}	V_{CC}=2V	200			ns
			V_{CC}=4.5V	40			ns
			V_{CC}=6V	34			ns

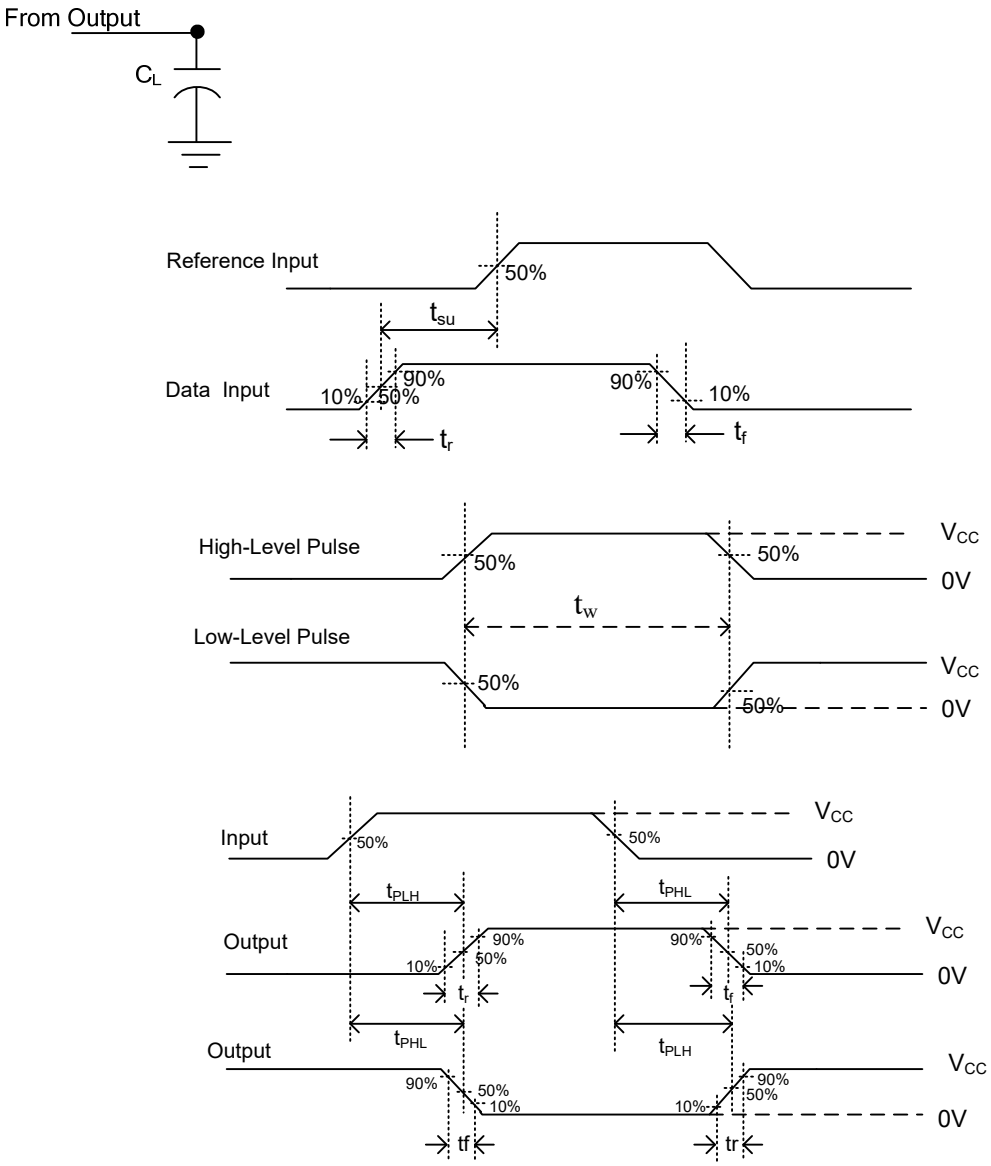
■ SWITCHING CHARACTERISTICS (C_L=50pF, T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Clock Pulse Frequency	f_{MAX}	V_{CC}=2V	4.3			MHz
		V_{CC}=4.5V	22			MHz
		V_{CC}=6V	25			MHz
Propagation Delay From CLKI to Q_D	t_{PD}	V_{CC}=2V			615	ns
		V_{CC}=4.5V			123	ns
		V_{CC}=6V			105	ns
Propagation Delay From CLR to Any Q	t_{PHL}	V_{CC}=2V			175	ns
		V_{CC}=4.5V			35	ns
		V_{CC}=6V			30	ns
Output Rise or Fall Time	t_t	V_{CC}=2V			95	ns
		V_{CC}=4.5V			19	ns
		V_{CC}=6V			16	ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	No load		88		pF

■ TEST CIRCUIT AND WAVEFORMS



Notes: 1. C_L=50pF, C_L includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics: P_{RR} ≤ 1MHz, Z_O = 50Ω, t_r ≤ 6ns, t_f ≤ 6ns.
3. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
4. t_{PLH} and t_{PHL} are the same as t_{PD}.