



80NM60-U2

Power MOSFET

80A, 600V N-CHANNEL SUPER-JUNCTION MOSFET

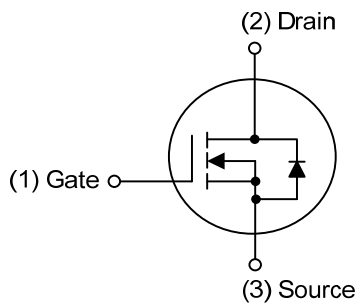
DESCRIPTION

The **UTC 80NM60-U2** is a Super Junction MOSFET Structure and is designed to have better characteristics, such as fast switching time, low gate charge, low on-state resistance and a high rugged avalanche characteristics. This power MOSFET is usually used at AC-DC converters for power applications.

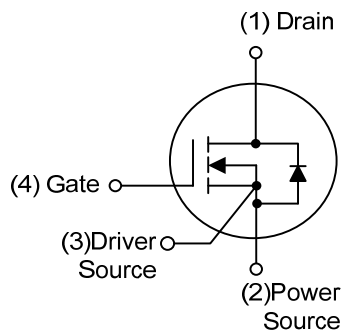
FEATURES

- * $R_{DS(ON)} \leq 42 \text{ m}\Omega$ @ $V_{GS}=10\text{V}$, $I_D=20\text{A}$
- * Fast switching capability
- * Avalanche energy tested
- * Improved dv/dt capability, high ruggedness

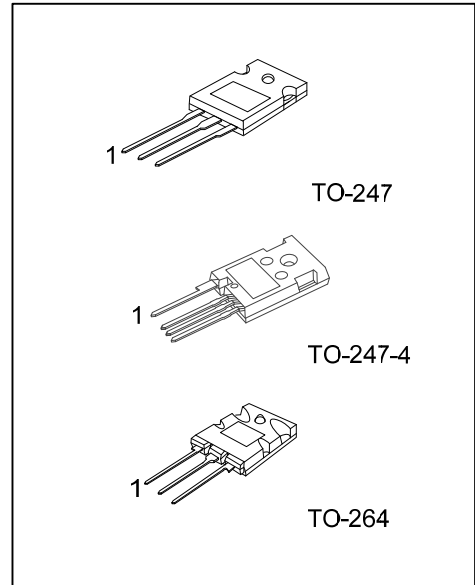
SYMBOL



TO-247 / TO-264



TO-247-4



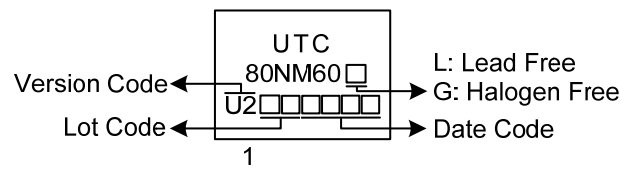
ORDERING INFORMATION

Ordering Number		Package	Pin Assignment				Packing
Lead Free	Halogen Free		1	2	3	4	
80NM60L-U2-T47-T	80NM60G-U2-T47-T	TO-247	G	D	S	-	Tube
80NM60L-U2-T474-T	80NM60G-U2-T474-T	TO-247-4	D	S	S	G	Tube
80NM60L-U2-T64-T	80NM60G-U2-T64-T	TO-264	G	D	S	-	Tube

Note: Pin Assignment: G: Gate D: Drain S: Source

80NM60G-U2-T47-T	(1)Packing Type	(1) T: Tube
	(2)Package Type	(2) T47: TO-247, T474: TO-247-4, T64: TO-264
	(3)Version Code	(3) Version U2
	(4)Green Package	(4) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING



■ ABSOLUTE MAXIMUM RATINGS ($T_c = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER		SYMBOL	RATINGS	UNIT
Drain-Source Voltage		V _{DSS}	600	V
Gate-Source Voltage		V _{GSS}	±30	V
Drain Current	Continuous	I _D	80	A
	Pulsed (Note 2)	I _{DM}	240	A
Avalanche Energy	Single Pulsed (Note 3)	E _{AS}	563	mJ
MOSFET dv/dt ruggedness		dv/dt	50	V/ns
Peak Diode Recovery dv/dt (Note 4)			7.7	V/ns
Power Dissipation	TO-247/TO-247-4	P _D	250	W
	TO-264		446	W
Junction Temperature		T _J	+150	°C
Storage Temperature Range		T _{STG}	-55 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged.

Absolute maximum ratings are stress ratings only and functional device operation is not implied.

2. Repetitive Rating: Pulse width limited by maximum junction temperature.

3. $L = 5\text{mH}$, $I_{AS} = 15\text{A}$, $V_{DD} = 50\text{V}$, $R_G = 25\Omega$, Starting $T_J = 25^\circ\text{C}$.

4. $I_{SD} \leq 30\text{A}$, $di/dt \leq 200\text{A}/\mu\text{s}$, $V_{DD} \leq V_{(BR)DSS}$, $T_J = 25^\circ\text{C}$.

■ THERMAL DATA

PARAMETER		SYMBOL	RATINGS	UNIT
Junction to Ambient		θ_{JA}	40	$^\circ\text{C}/\text{W}$
Junction to Case	TO-247/TO-247-4	θ_{JC}	0.5	$^\circ\text{C}/\text{W}$
	TO-264		0.28	$^\circ\text{C}/\text{W}$

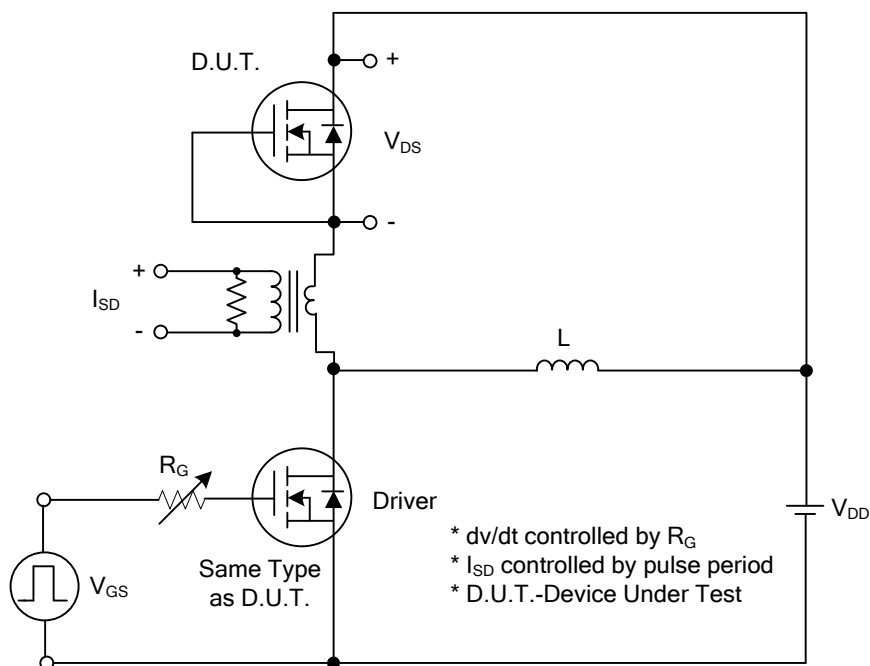
■ ELECTRICAL CHARACTERISTICS (T_J=25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =250μA	600			V
Drain-Source Leakage Current	I _{DSS}	V _{DS} =600V, V _{GS} =0V			10	μA
Gate-Source Leakage Current	I _{GSS}	V _{DS} =0V ,V _{GS} =±30V			±100	nA
ON CHARACTERISTICS						
Gate Threshold Voltage	V _{GS(TH)}	V _{DS} = V _{GS} , I _D = 250μA	2.5		4.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} = 10V, I _D = 20A			42	mΩ
DYNAMIC PARAMETERS						
Input Capacitance	C _{ISS}	V _{GS} =0V, V _{DS} =50V, f=1.0MHz		5898		pF
Output Capacitance	C _{OSS}			2383		pF
Reverse Transfer Capacitance	C _{RSS}			106		pF
SWITCHING PARAMETERS						
Total Gate Charge (Note 1)	Q _G	V _{DS} =480V, V _{GS} =10V, I _D =80A (Note 1, 2)		303		nC
Gate to Source Charge	Q _{GS}			61		nC
Gate to Drain Charge	Q _{GD}			167		nC
Turn-ON Delay Time (Note 1)	t _{D(ON)}	V _{DD} =100V, V _{GS} =10V, I _D =80A, R _G =25Ω (Note 1, 2)		106		ns
Rise Time	t _R			178		ns
Turn-OFF Delay Time	t _{D(OFF)}			311		ns
Fall-Time	t _F			93		ns
SOURCE- DRAIN DIODE RATINGS AND CHARACTERISTICS						
Maximum Body-Diode Continuous Current	I _S				80	A
Maximum Body-Diode Pulsed Current	I _{SM}				240	A
Drain-Source Diode Forward Voltage (Note 1)	V _{SD}	I _S =80A, V _{GS} =0V			1.4	V
Body Diode Reverse Recovery Time (Note 1)	t _{rr}	I _S =30A, V _{GS} =0V,		804		ns
Body Diode Reverse Recovery Charge	Q _{rr}	dl _F /dt=100A/μs		19		μC

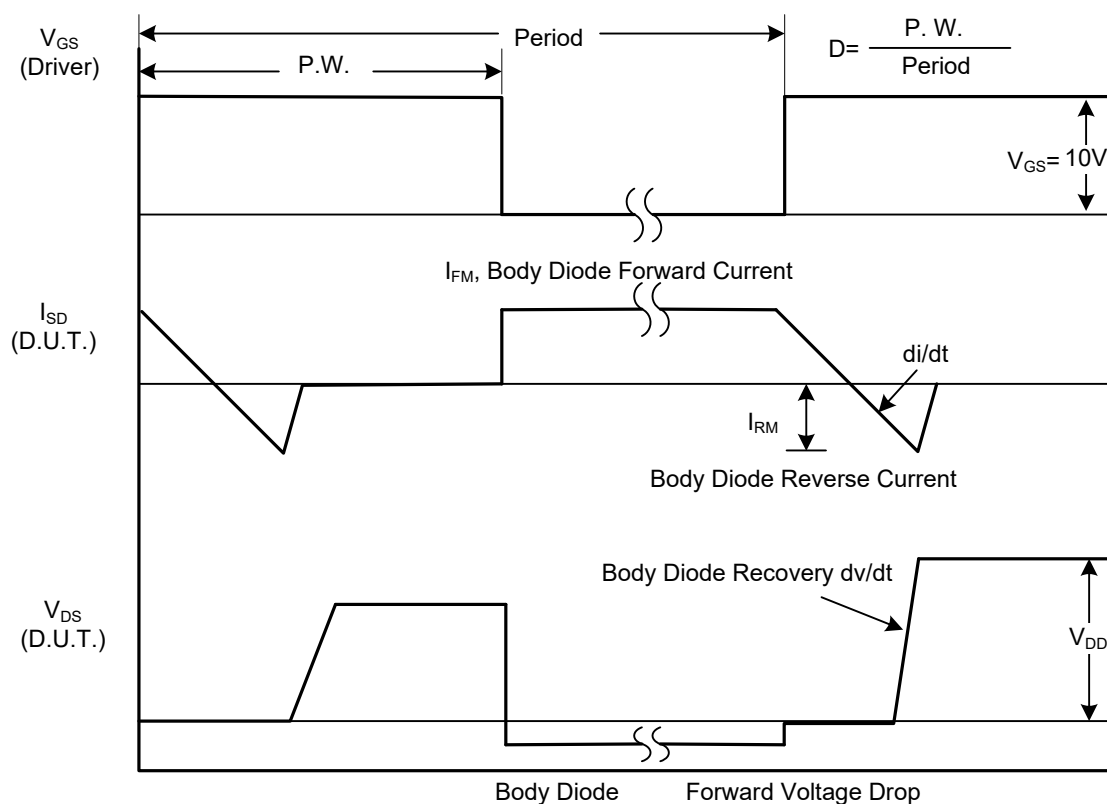
Notes: 1. Pulse Test: Pulse width ≤ 300μs, Duty cycle ≤ 2%.

2. Essentially independent of operating temperature.

■ TEST CIRCUITS AND WAVEFORMS

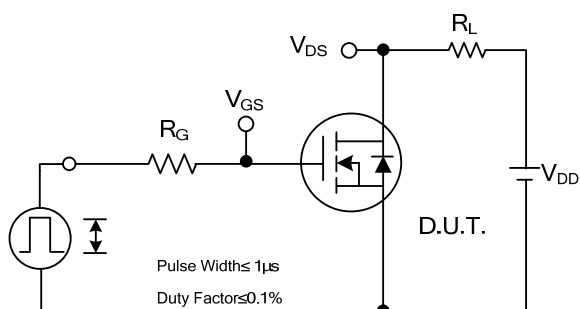


Peak Diode Recovery dv/dt Test Circuit

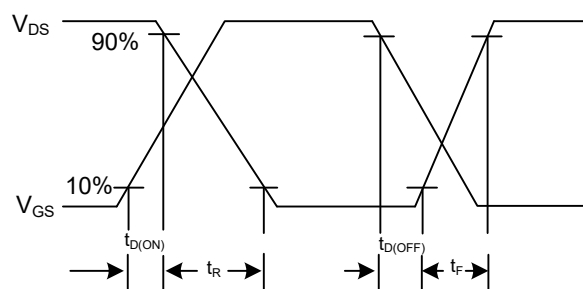


Peak Diode Recovery dv/dt Waveforms

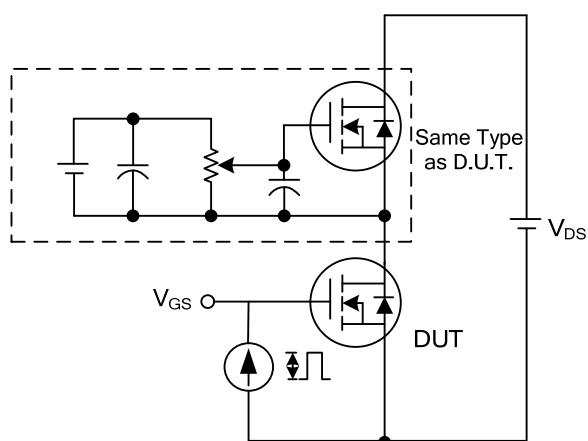
■ TEST CIRCUITS AND WAVEFORMS (Cont.)



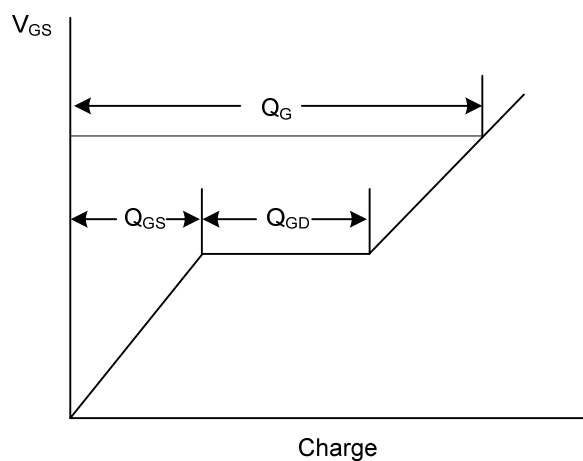
Switching Test Circuit



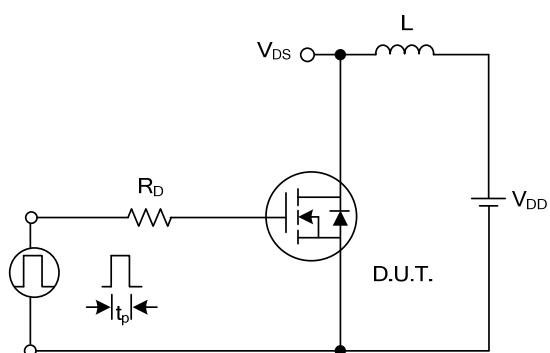
Switching Waveforms



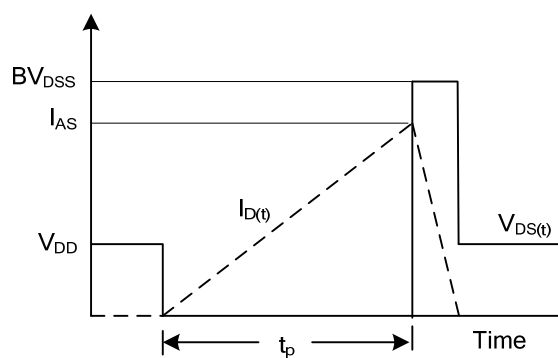
Gate Charge Test Circuit



Gate Charge Waveform

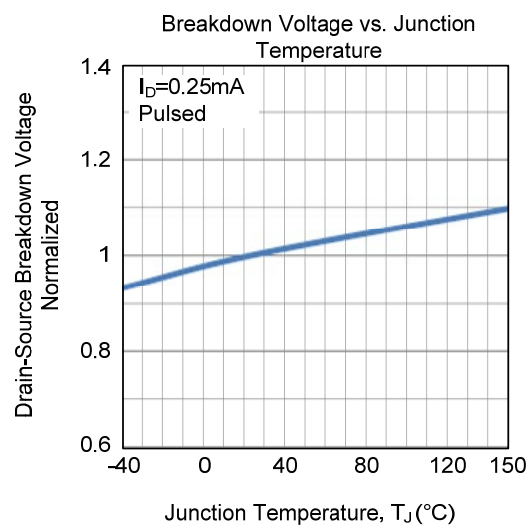
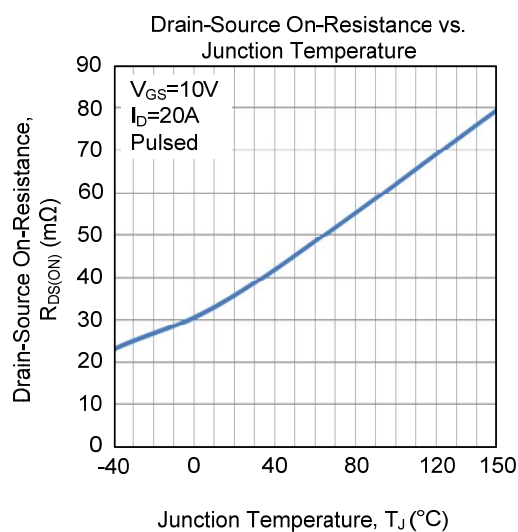
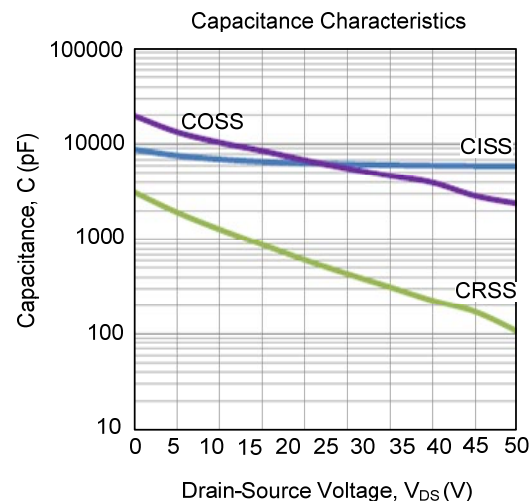
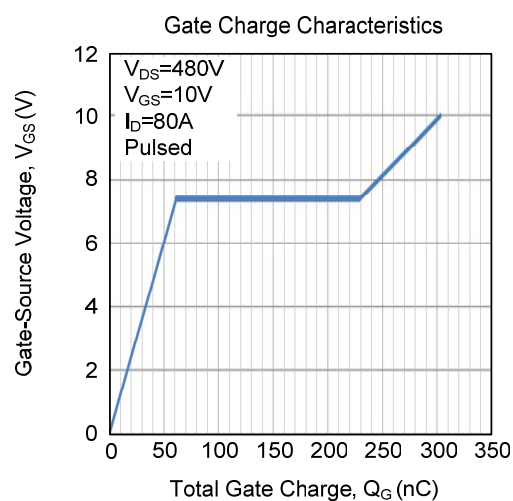
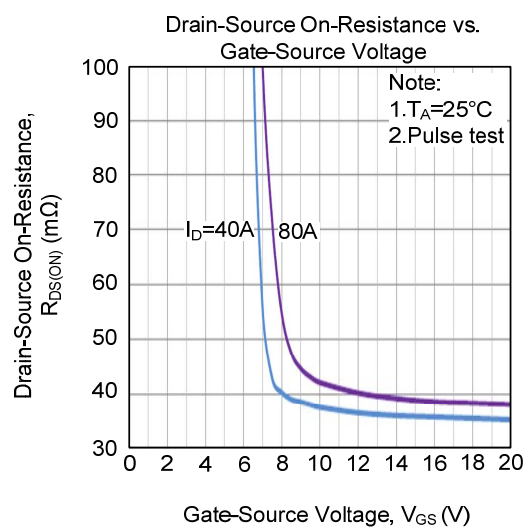
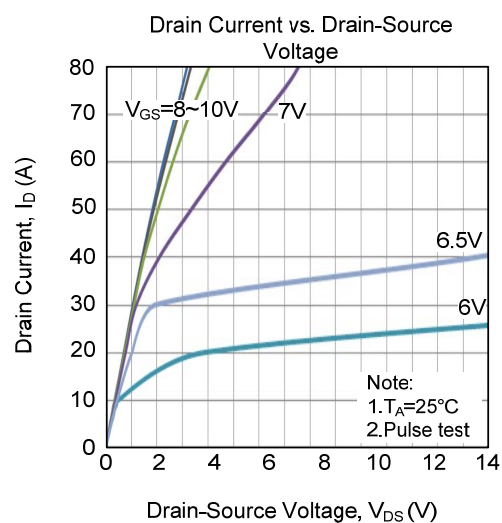


Unclamped Inductive Switching Test Circuit

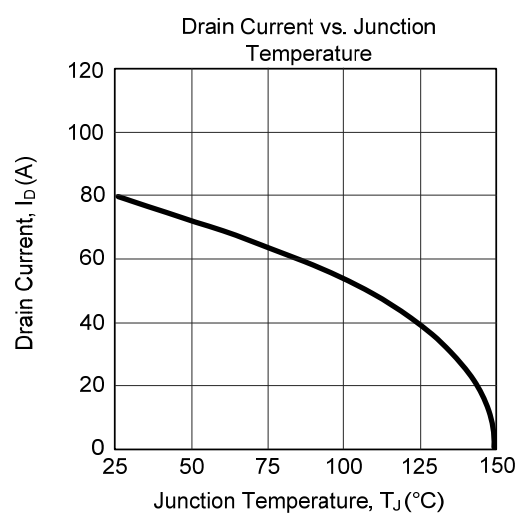
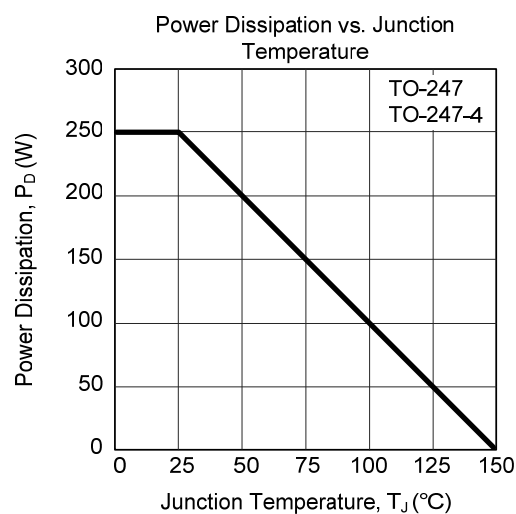
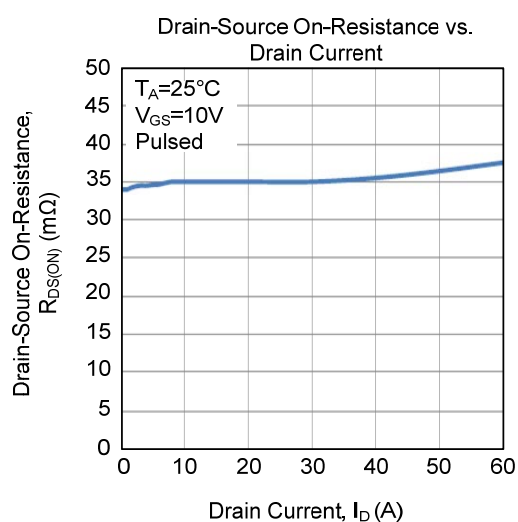
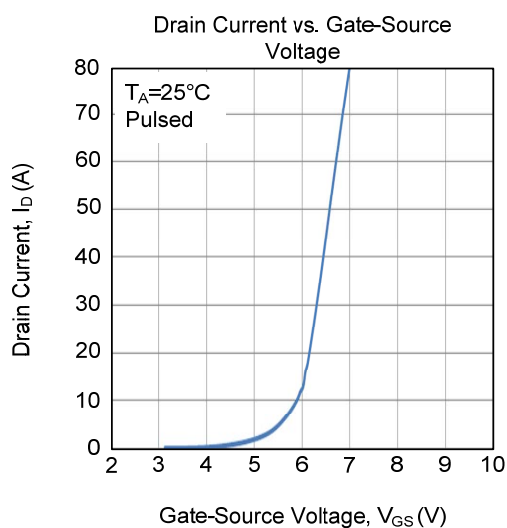
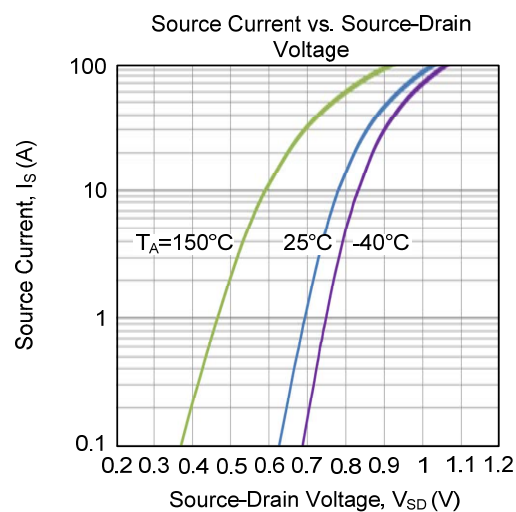
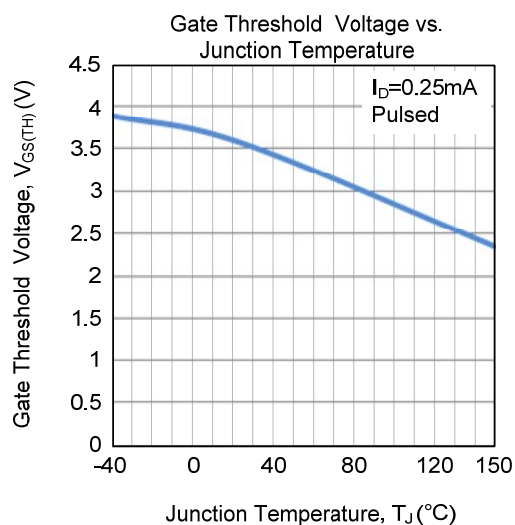


Unclamped Inductive Switching Waveforms

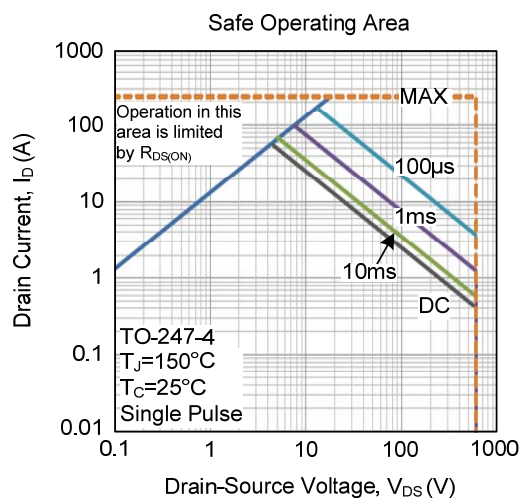
TYPICAL CHARACTERISTICS



■ TYPICAL CHARACTERISTICS (Cont.)



■ TYPICAL CHARACTERISTICS (Cont.)



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