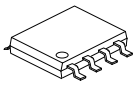
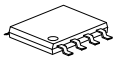
DUAL-BIT DUAL SUPPLY, BUS TRANSCEIVER WITH CONFIGURABLE LEVEL-SHIFTING AND TRANSLATION



SOP-8



TSSOP-8

■ DESCRIPTION

This 2-bit non-inverting bus transceiver uses two separate configurable power-supply rails. The A ports are designed to track V_{CCA} and accepts any supply Voltage from 1.2V to 3.6V. The B ports are designed to track V_{CCB} and accepts any supply Voltage from 1.2V to 3.6V. This allows for universal low Voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V Voltage nodes.

The **U74AVC2T45** is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR pin) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess leakage current on the internal CMOS structure.

■ FEATURES

* V_{CC} Isolation Feature: If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
* Dual Supply Rail Design
* I/Os Are 4.6V Over Voltage Tolerant
* I_{OFF} Supports Partial-Power-Down Mode Operation

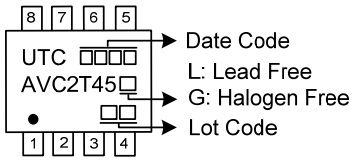
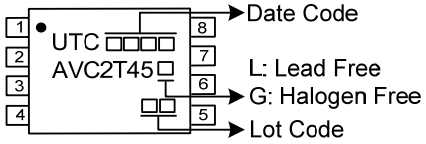
■ RDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74AVC2T45L-S08-R	U74AVC2T45G-S08-R	SOP-8	Tape Reel
U74AVC2T45L-P08-R	U74AVC2T45G-P08-R	TSSOP-8	Tape Reel

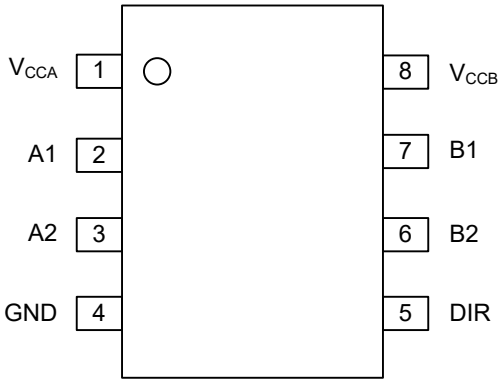
U74AVC2T45G-S08-R
(1)Packing Type
(2)Package Type
(3)Green Package

(1) R: Tape Reel
(2) S08: SOP-8, P08: TSSOP-8
(3) G: Halogen Free and Lead Free, L: Lead Free

■ MARKING

SOP-8	TSSOP-8
	

■ PIN CONFIGURATION



■ PIN DESCRIPTION

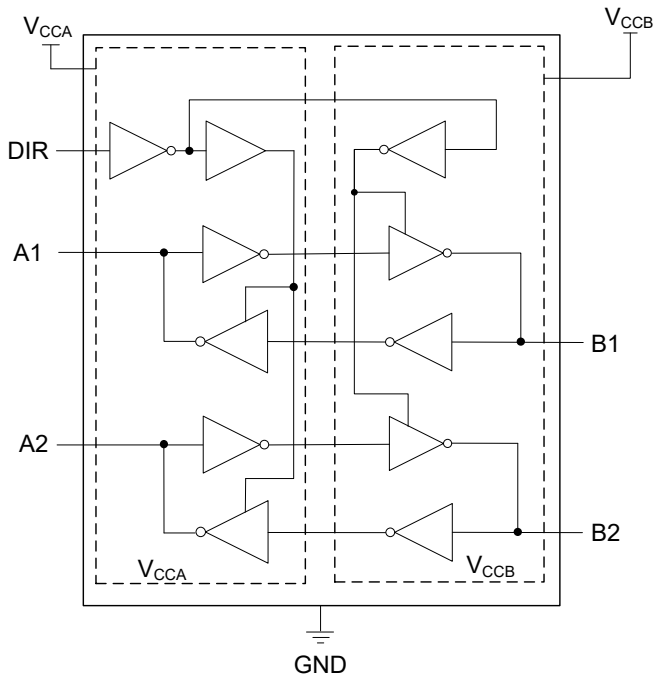
PIN NO.	PIN NAME	I/O	DESCRIPTION
1	V_{CCA}	P	Supply Voltage A
2	A1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
3	A2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA}.
4	GND	G	Ground
5	DIR	I	Direction Pin, Connect to GND or to V_{CCA}
6	B2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
7	B1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB}.
8	V_{CCB}	P	Supply Voltage B

Note: P=Power, G=Ground, I/O=Input and output, I=Input.

■ FUNCTION TABLE

INPUTS DIR	OPERATION
L	B data to A bus
H	A data to B bus

■ LOGIC DIAGRAM (POSITIVE LOGIC)



■ ABSOLUTE MAXIMUM RATING (Unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	RATINGS	UNIT
Supply Voltage	V_{CCA}		-0.5 ~ 4.6	V
Supply Voltage	V_{CCB}		-0.5 ~ 4.6	V
Input Voltage (Note 2)	V_{IN}	A Port	-0.5 ~ 4.6	V
		B Port	-0.5 ~ 4.6	V
		Control Input	-0.5 ~ 4.6	V
Voltage applied to any output in the high-impedance or power off state (Note 2)	V_{OUT}	A Port	-0.5 ~ 4.6	V
		B Port	-0.5 ~ 4.6	V
Voltage applied to any output in the high or low state (Note 2, 3)	V_{OUT}	A Port	-0.5 ~ V_{CCA}+0.5	V
		B Port	-0.5 ~ V_{CCB}+0.5	V
Continuous Output Current	I_{OUT}		±50	mA
Continuous current through V_{CCA}, V_{CCB} or GND			±100	mA
Input Clamp Current	I_{IK}	V_{IN}<0V	-50	mA
Output Clamp Current	I_{OK}	V_{OUT}<0V	-50	mA
Storage Temperature Range	T_{STG}		-65 ~ +150	°C

Notes: 1. Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.
2. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
3. The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current ratings are observed.

■ RECOMMENDED OPERATING CONDITIONS

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage		V_{CCA}		1.2		3.6	V
Supply Voltage		V_{CCB}		1.2		3.6	V
High-Level Input Voltage	Data Inputs (Note 1)	V_{IH}	V_{CCI}=1.2V~1.95V	V_{CCI} (Note 4) ×0.65			V
			V_{CCI}=1.95V~2.7V	1.6			V
			V_{CCI}=2.7V~3.6V	2			V
	DIR (Referenced to V_{CCA}) (Note 2)		V_{CCI}=1.2V~1.95V	V_{CCA} ×0.65			V
			V_{CCI}=1.95V~2.7V	1.6			V
			V_{CCI}=2.7V~3.6V	2			V
Low-Level Input Voltage	Data Inputs (Note 1)	V_{IL}	V_{CCI}=1.2V~1.95V			V_{CCI} (Note 4) ×0.35	V
			V_{CCI}=1.95V~2.7V			0.7	V
			V_{CCI}=2.7V~3.6V			0.8	V
	DIR (Referenced to V_{CCA}) (Note 2)		V_{CCI}=1.2V~1.95V			V_{CCA} ×0.35	V
			V_{CCI}=1.95V~2.7V			0.7	V
			V_{CCI}=2.7V~3.6V			0.8	V
Input Voltage		V_{IN}		0		3.6	V
Output Voltage	Active State	V_{OUT}		0		V_{CCO} (Note 4)	V
	3-State			0		3.6	V
Input Transition Rise or Fall Rate		Δt/Δv				5	ns/V
Operating Temperature		T_A		-40		+125	°C

Notes: 1. For V_{CCI} values not specified in the data sheet, V_{IH} min=V_{CCI}×0.7V,V_{IL} max=V_{CCI}×0.3V.
2. For V_{CCI} values not specified in the data sheet, V_{IH} min=V_{CCA}×0.7V,V_{IL} max=V_{CCA}×0.3V.
3. V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB}.
4. V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB}.

■ ELECTRICAL CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output High Voltage	V_{OH}	V_I=V_{IH}	V_{CCA}=1.2V~3.6V, V_{CCB}=1.2V~3.6V, I_{OH}=-100μA	V_{CCO}-0.2			V
			V_{CCA}=1.2V, V_{CCB}=1.2V, I_{OH}=-3mA		0.95		V
			V_{CCA}=1.4V, V_{CCB}=1.4V, I_{OH}=-6mA	1.05			V
			V_{CCA}=1.65V, V_{CCB}=1.65V, I_{OH}=-8mA	1.2			V
			V_{CCA}=2.3V, V_{CCB}=2.3V, I_{OH}=-9mA	1.75			V
			V_{CCA}=3V, V_{CCB}=3V, I_{OH}=-12mA	2.3			V

■ ELECTRICAL CHARACTERISTICS (Cont.)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output Low Voltage		V_{OL}	$V_I=V_{IL}$	V_{CCA}=1.2V~3.6V, V_{CCB}=1.2V~3.6V, I_{OL}=100μA			0.2	V
				V_{CCA}=1.2V, V_{CCB}=1.2V, I_{OL}=3mA		0.25		V
				V_{CCA}=1.4V, V_{CCB}=1.4V, I_{OL}=6mA			0.35	V
				V_{CCA}=1.65V, V_{CCB}=1.65V, I_{OL}=8mA			0.45	V
				V_{CCA}=2.3V, V_{CCB}=2.3V, I_{OL}=9mA			0.55	V
				V_{CCA}=3V, V_{CCB}=3V, I_{OL}=12mA			0.7	V
Input Leakage Current	DIR	$I_{I(LEAK)}$	$V_{IN}=V_{CCA}$ or GND, V_{CCA}=1.2V~3.6V, V_{CCB}=1.2V~3.6V			±0.025	±0.25	μA
Power OFF Leakage Current	A Port	I_{OFF}	V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V, V_{CCB}=0V~3.6V			±0.1	±1	μA
	B Port		V_{IN} or V_{OUT}=0~3.6V, V_{CCA}=0V~3.6V, V_{CCB}=0V			±0.1	±1	μA
Output OFF-State Current	A Port	I_{OZ}	$V_{OUT}=V_{CCO}$ or GND, $V_{IN}=V_{CCI}$ or GND, V_{CCA}=3.6V, V_{CCB}=0V			±0.5	±2.5	μA
	B Port		$V_{OUT}=V_{CCO}$ or GND, $V_{IN}=V_{CCI}$ or GND, V_{CCA}=0V, V_{CCB}=3.6V			±0.5	±2.5	μA
Supply A Current		I_{CCA}	$V_{IN}=V_{CCI}$ or GND, I_{OUT}=0A	V_{CCA}=1.2V~3.6V, V_{CCA}=1.2V~3.6V			10	μA
				V_{CCA}=0V, V_{CCB}=3.6V			-2	μA
				V_{CCA}=3.6V, V_{CCB}=0V			10	μA
Supply B Current		I_{CCB}		V_{CCA}=1.2V~3.6V, V_{CCA}=1.2V~3.6V			10	μA
				V_{CCA}=0V, V_{CCB}=3.6V			10	μA
				V_{CCA}=3.6V, V_{CCB}=0V			-2	μA
Supply A Current & Supply B Current		$I_{CCA}+I_{CCB}$		V_{CCA}=1.2V~3.6V, V_{CCB}=1.2V~3.6V			20	μA
Input Capacitance	Control Inputs	C_{IN}	V_{IN}=3.3V or GND, V_{CCA}=3.3V, V_{CCB}=3.3V			2.5		pF
Output Capacitance	A or B Port	C_{IO}	V_{OUT}=3.3V or GND, V_{CCA}=3.3V, V_{CCB}=3.3V			6		pF

Notes: 1. V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB}.
2. V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB}.

■ SWITCHING CHARACTERISTICS (Unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (A) to Output (B)	t_{PLH} t_{PHL}	V_{CCA}=1.2V	V_{CCB}=1.2V		4.1		ns
			V_{CCB}=1.5V		3.6		ns
			V_{CCB}=1.8V		3.4		ns
			V_{CCB}=2.5V		3.2		ns
			V_{CCB}=3.3V		3.2		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		2.8		ns
			V_{CCB}=1.5V	0.7		5.4	ns
			V_{CCB}=1.8V	0.5		4.6	ns
			V_{CCB}=2.5V	0.4		3.7	ns
			V_{CCB}=3.3V	0.3		3.5	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		3.7		ns
			V_{CCB}=1.5V	0.5		5.2	ns
			V_{CCB}=1.8V	0.4		4.3	ns
			V_{CCB}=2.5V	0.2		3.4	ns
			V_{CCB}=3.3V	0.2		3.1	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		3.6		ns
			V_{CCB}=1.5V	0.4		4.9	ns
			V_{CCB}=1.8V	0.2		4.0	ns
			V_{CCB}=2.5V	0.2		3.0	ns
			V_{CCB}=3.3V	0.2		2.6	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		3.2		ns
			V_{CCB}=1.5V	0.3		4.7	ns
			V_{CCB}=1.8V	0.2		3.8	ns
			V_{CCB}=2.5V	0.2		2.8	ns
			V_{CCB}=3.3V	0.2		2.4	ns
Propagation Delay From Input (B) to Output (A)	t_{PLH} t_{PHL}	V_{CCA}=1.2V	V_{CCB}=1.2V		4.4		ns
			V_{CCB}=1.5V		4.1		ns
			V_{CCB}=1.8V		4.0		ns
			V_{CCB}=2.5V		3.9		ns
			V_{CCB}=3.3V		3.9		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		3.7		ns
			V_{CCB}=1.5V	0.8		5.4	ns
			V_{CCB}=1.8V	0.7		5.2	ns
			V_{CCB}=2.5V	0.6		4.9	ns
			V_{CCB}=3.3V	0.5		4.7	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		3.4		ns
			V_{CCB}=1.5V	0.7		4.7	ns
			V_{CCB}=1.8V	0.5		4.4	ns
			V_{CCB}=2.5V	0.5		4.0	ns
			V_{CCB}=3.3V	0.4		3.8	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		3.1		ns
			V_{CCB}=1.5V	0.6		3.8	ns
			V_{CCB}=1.8V	0.5		3.4	ns
			V_{CCB}=2.5V	0.4		3.0	ns
			V_{CCB}=3.3V	0.3		2.8	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		4.4		ns
			V_{CCB}=1.5V	0.6		3.6	ns
			V_{CCB}=1.8V	0.4		3.1	ns
			V_{CCB}=2.5V	0.3		2.6	ns
			V_{CCB}=3.3V	0.3		2.4	ns

■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (DIR) to Output (A)	t_{PHZ} t_{PLZ}	V_{CCA}=1.2V	V_{CCB}=1.2V		6.2		ns
			V_{CCB}=1.5V		6.2		ns
			V_{CCB}=1.8V		6.2		ns
			V_{CCB}=2.5V		6.0		ns
			V_{CCB}=3.3V		5.8		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		4.9		ns
			V_{CCB}=1.5V	1.3		8.5	ns
			V_{CCB}=1.8V	1.3		7.8	ns
			V_{CCB}=2.5V	1.1		7.7	ns
			V_{CCB}=3.3V	1.4		7.6	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		4.7		ns
			V_{CCB}=1.5V	1.3		8.1	ns
			V_{CCB}=1.8V	0.7		6.9	ns
			V_{CCB}=2.5V	1.4		5.3	ns
			V_{CCB}=3.3V	1.1		5.2	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		3.4		ns
			V_{CCB}=1.5V	0.7		7.9	ns
			V_{CCB}=1.8V	0.8		6.4	ns
			V_{CCB}=2.5V	0.8		5	ns
			V_{CCB}=3.3V	0.5		4.3	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		3.9		ns
			V_{CCB}=1.5V	1.1		8	ns
			V_{CCB}=1.8V	1		6.5	ns
			V_{CCB}=2.5V	1.3		4.7	ns
			V_{CCB}=3.3V	1.2		4	ns
Propagation Delay From Input (DIR) to Output (B)	t_{PHZ} t_{PLZ}	V_{CCA}=1.2V	V_{CCB}=1.2V		6.0		ns
			V_{CCB}=1.5V		5.0		ns
			V_{CCB}=1.8V		4.8		ns
			V_{CCB}=2.5V		3.8		ns
			V_{CCB}=3.3V		3.2		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		5.7		ns
			V_{CCB}=1.5V	1.1		7.0	ns
			V_{CCB}=1.8V	1.4		6.9	ns
			V_{CCB}=2.5V	1.2		6.9	ns
			V_{CCB}=3.3V	1.7		7.1	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		5.4		ns
			V_{CCB}=1.5V	1.3		5.8	ns
			V_{CCB}=1.8V	1.3		5.9	ns
			V_{CCB}=2.5V	0.8		5.7	ns
			V_{CCB}=3.3V	1.5		5.9	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		4.8		ns
			V_{CCB}=1.5V	1.0		4.3	ns
			V_{CCB}=1.8V	0.6		4.3	ns
			V_{CCB}=2.5V	0.5		4.2	ns
			V_{CCB}=3.3V	1.1		4.1	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		4.4		ns
			V_{CCB}=1.5V	0.5		6.6	ns
			V_{CCB}=1.8V	0.3		5.6	ns
			V_{CCB}=2.5V	0.3		4.6	ns
			V_{CCB}=3.3V	1.1		4.2	ns

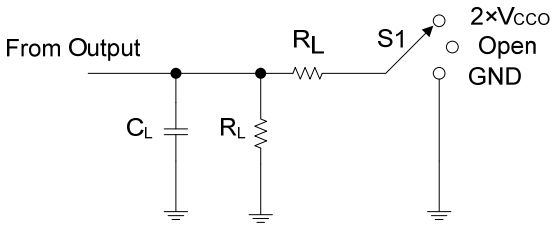
■ SWITCHING CHARACTERISTICS (Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Propagation Delay From Input (DIR) to Output (A)	t_{PZH} t_{PZL}	V_{CCA}=1.2V	V_{CCB}=1.2V		10		ns
			V_{CCB}=1.5V		8.1		ns
			V_{CCB}=1.8V		7.8		ns
			V_{CCB}=2.5V		6.7		ns
			V_{CCB}=3.3V		7.1		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		8.4		ns
			V_{CCB}=1.5V			12.4	ns
			V_{CCB}=1.8V			12.1	ns
			V_{CCB}=2.5V			11.8	ns
			V_{CCB}=3.3V			11.8	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		7.8		ns
			V_{CCB}=1.5V			10.5	ns
			V_{CCB}=1.8V			10.3	ns
			V_{CCB}=2.5V			9.7	ns
			V_{CCB}=3.3V			9.7	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		6.9		ns
			V_{CCB}=1.5V			8.5	ns
			V_{CCB}=1.8V			7.7	ns
			V_{CCB}=2.5V			7.2	ns
			V_{CCB}=3.3V			6.9	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		5.5		ns
			V_{CCB}=1.5V			10.2	ns
			V_{CCB}=1.8V			8.7	ns
			V_{CCB}=2.5V			7.2	ns
			V_{CCB}=3.3V			6.6	ns
Propagation Delay From Input (DIR) to Output (B)	t_{PZH} t_{PZL}	V_{CCA}=1.2V	V_{CCB}=1.2V		10		ns
			V_{CCB}=1.5V		8.8		ns
			V_{CCB}=1.8V		8.5		ns
			V_{CCB}=2.5V		8.2		ns
			V_{CCB}=3.3V		8.0		ns
		V_{CCA}=1.5V±0.1V	V_{CCB}=1.2V		7.7		ns
			V_{CCB}=1.5V			13.9	ns
			V_{CCB}=1.8V			12.4	ns
			V_{CCB}=2.5V			11.4	ns
			V_{CCB}=3.3V			11.1	ns
		V_{CCA}=1.8V±0.15V	V_{CCB}=1.2V		6.9		ns
			V_{CCB}=1.5V			13.3	ns
			V_{CCB}=1.8V			11.2	ns
			V_{CCB}=2.5V			8.7	ns
			V_{CCB}=3.3V			8.3	ns
		V_{CCA}=2.5V±0.2V	V_{CCB}=1.2V		6.0		ns
			V_{CCB}=1.5V			12.8	ns
			V_{CCB}=1.8V			10.4	ns
			V_{CCB}=2.5V			8.0	ns
			V_{CCB}=3.3V			6.9	ns
		V_{CCA}=3.3V±0.3V	V_{CCB}=1.2V		6.4		ns
			V_{CCB}=1.5V			12.7	ns
			V_{CCB}=1.8V			10.3	ns
			V_{CCB}=2.5V			7.5	ns
			V_{CCB}=3.3V			6.4	ns

■ OPERATING CHARACTERISTICS (Unless otherwise specified)

PARAMETER		SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	A Port Input B Port Output	C_{PDA}	C_L=0, f=10MHz t_r=t_f=1nS	V_{CCB}=1.2V		3		pF
				V_{CCB}=1.5V		3		pF
				V_{CCB}=1.8V		3		pF
				V_{CCB}=2.5V		3		pF
				V_{CCB}=3.3V		4		pF
	B Port Input A Port Output			V_{CCB}=1.2V		12		pF
				V_{CCB}=1.5V		13		pF
				V_{CCB}=1.8V		13		pF
				V_{CCB}=2.5V		14		pF
				V_{CCB}=3.3V		15		pF
	A Port Input B Port Output	C_{PDB}		V_{CCB}=1.2V		12		pF
				V_{CCB}=1.5V		13		pF
				V_{CCB}=1.8V		13		pF
				V_{CCB}=2.5V		14		pF
				V_{CCB}=3.3V		15		pF
	B Port Input A Port Output			V_{CCB}=1.2V		3		pF
				V_{CCB}=1.5V		3		pF
				V_{CCB}=1.8V		3		pF
				V_{CCB}=2.5V		3		pF
				V_{CCB}=3.3V		4		pF

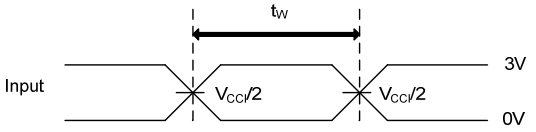
■ TEST CIRCUIT AND WAVEFORMS



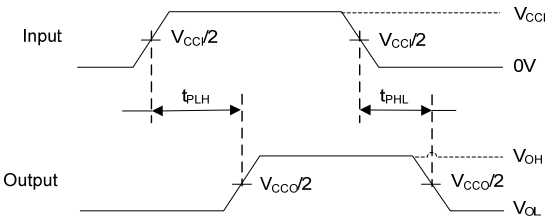
TEST	S1
t_{PD}	Open
t_{PLZ}/t_{PZL}	2×V_{CCO}
t_{PHZ}/t_{PZH}	GND

LOAD CIRCUIT

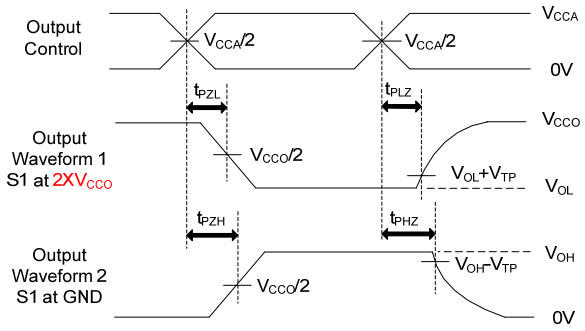
V_{CCO}	C_L	R_L	V_{TP}
1.2V	15pF	2kΩ	0.1V
1.5V±0.1V	15pF	2kΩ	0.1V
1.8V±0.15V	15pF	2kΩ	0.15V
2.5V±0.2V	15pF	2kΩ	0.15V
3.3V±0.3V	15pF	2kΩ	0.3V



PULSE DURATION



PROPAGATION DELAY TIMES



ENABLE AND DISABLE TIMES

Note: C_L includes probe and jig capacitance.

■ DETAILED DESCRIPTION

Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2V to 3.6V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2V to 3.6V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V voltage nodes.

The **U74AVC2T45** is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

The **U74AVC2T45** is designed so that the DIR input is powered by supply voltage from V_{CCA}.

This device is fully specified for partial-power-down applications using off output current (I_{OFF}). The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both ports are put in a high-impedance state. This will prevent a false high or low logic being presented at the output.

■ FEATURES DESCRIPTION

VCC Isolation

The V_{CC} isolation feature ensures that if either V_{CCA} or V_{CCB} are at GND, both ports will be in a high-impedance state (I_{OZ} shown in Electrical Characteristics). This prevents false logic levels from being presented to either bus.

2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2V to 3.6V power-supply range.

IO Ports are 4.6V Tolerant

The IO ports are up to 4.6V tolerant.

Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{OFF}). The I_{OFF} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

■ TYPICAL APPLICATION CIRCUIT